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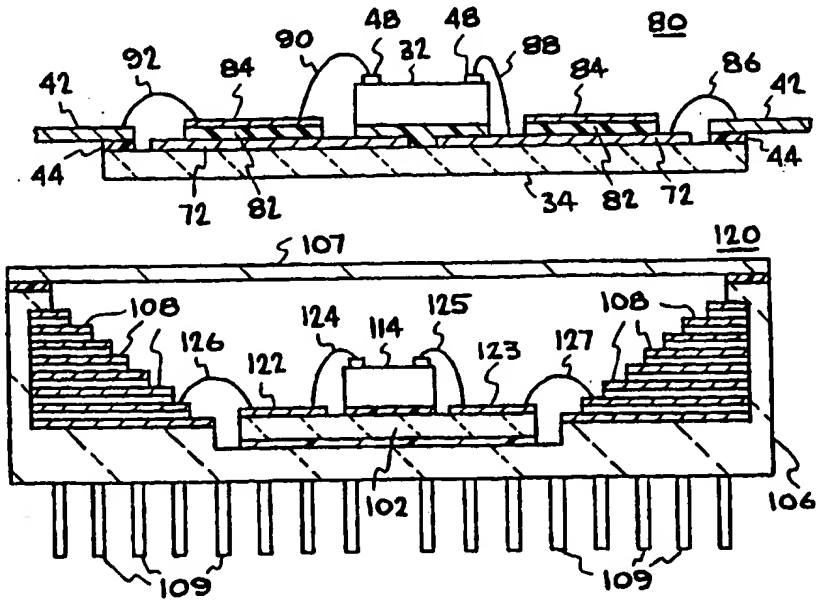
(54) Title: ELECTRICALLY AND THERMALLY ENHANCED PACKAGE USING A SEPARATE SILICON SUBSTRATE

(57) Abstract




An integrated-circuit package assembly includes a separate silicon substrate (34) to which an integrated-circuit die (32) is fixed. The separate silicon substrate (34) serves as a heat spreader for the integrated-circuit die (32). The separate silicon substrate (34) to which the integrated-circuit die (32) is fixed is packaged in either a molded package body (80) or a cavity-type package body (120). For the molded package body (80), the package body is molded around a leadframe (42), the integrated-circuit die (32), and the separate silicon substrate (34) to which the integrated-circuit die (32) is fixed. For a molded package body (80), the leadframe (42) has bonding fingers formed at the inward ends thereof which are attached to the separate silicon substrate (34) or the leadframe may have a die-attach pad (20) to which is fixed the separate silicon substrate (34). For the cavity-type package (120), the package body includes a mounting surface formed adjacent to a cavity formed therein and the mounting surface has the separate silicon substrate (102) fixed to the top surface thereof. The cavity-type body (120) is formed of a ceramic material or as a multi-layer pringed-circuit board. One or more interposer areas (122) are formed on the top surface of the silicon substrate (102) for attachment of connection wires (125, 127) from the integrated-circuit die (114) or the leadframe (42). A portion of the interposer (72, 122) can extend between the integrated circuit die (32, 114) and the top surface of the silicon substrate (34, 102) to accomodate integrated-circuit dies (32, 114) of various sizes. The interposer includes a layer of oxide (82) formed on the surface of the silicon substrate (34, 102), which layer of oxide is covered with a layer of conductive material (84).

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# ELECTRICALLY AND THERMALLY ENHANCED PACKAGE USING A SEPARATE SILICON SUBSTRATE

## BACKGROUND OF THE INVENTION

1. Technical Field . This invention relates to integrated-circuit packages and, more particularly, to techniques for cooling integrated-circuit packages.

2. Background of Invention. Previously, power and ground planes have been added to molded-plastic and hermetically-sealed integrated-circuit packages to improve the electrical performance of these packages. The added power and ground planes provided improved electrical performance by lowering the inductance of the power and ground leads. Additional power and ground planes are provided by using multi-layer leadframes and/or multi-layer printed-circuit-board substrates.

To improve the thermal performance of an integrated-circuit package, heatsinks are added either internally or externally to the packages. Adding a heatsink to an electrically enhanced package, as described above, provides an integrated-circuit package with both improved electrical performance and with improved thermal performance.

These prior packaging techniques for improving electrical and/or thermal performance tend to be expensive, consume large amounts of production time, and may present reliability problems due to thermal mismatches. Prior art

thermally conductive heatsink materials, such as copper, aluminum, alumina nitride, and multi-layer printed-circuit boards, are costly.

The need has arisen for an integrated-circuit package configuration which incorporates a cost effective heatsink or heat spreader material into the designs of plastic or cavity-type packages for integrated-circuits.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide an integrated-circuit package configuration for either plastic packages or for cavity-type packages which incorporates a cost effective heatsink or heat spreader material .

In accordance with this and other object of the invention, an integrated-circuit package assembly is provided for an integrated-circuit die. The package assembly is for various types of packages includes molded plastic packages and cavity-type packages, formed of materials such as ceramic or multi-layer printed-circuit board materials.

An important element of a package according to the invention is a separate and distinct silicon substrate. The separate silicon substrate has a top surface and a bottom surface with the integrated-circuit die being fixed to the top surface of the separate silicon substrate. The separate silicon substrate serves as a heat spreader for the integrated-circuit die to diffuse heat away from the integrated-circuit die.

The separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate can be packaged in several different types of package bodies, such as, for example, molded plastic packages and cavity-type packages,

formed of materials such as ceramic or multi-layer printed-circuit boards.

For the molded package body, the molded package body is formed around a leadframe, the integrated-circuit die, and the separate silicon substrate to which the integrated-circuit die is fixed. The leadframe has leads extending inwardly towards a central region of the leadframe and bonding fingers are formed at the inward ends of the leads. For a lead frame without a die-attach paddle, the bonding fingers are attached directly to the margins of the separate silicon substrate. Where the lead frame has a die-attach paddle, the separate silicon substrate is fixed to the bottom side of the die-attach paddle and the integrated-circuit die is fixed to the top side of the die-attach paddle.

Where the separate silicon substrate has lateral dimensions greater than the lateral dimensions of the integrated-circuit die, one or more interposer areas are formed on the top surface of the silicon substrate for attachment of connection wires from the integrated-circuit die or the leadframe. A portion of the interposer is formed on the top surface of the separate silicon substrate and extends between the integrated circuit die and the top surface of the silicon substrate to accommodate integrated-circuit dies of various sizes. The interposer is formed, for example, on the surface of the silicon substrate as a layer of oxide which is covered with a layer of conductive material.

For the cavity-type package body with a cavity formed therein, the package body includes a mounting surface formed adjacent to the cavity. The mounting surface has the separate silicon substrate fixed to the top surface thereof.

A method is provided for cooling an integrated-circuit die. The method includes fixing an integrated circuit die to the

top surface of a separate silicon substrate having a top surface and a bottom surface; packaging the separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate in a package body; and conducting heat from the integrated-circuit die using a separate silicon substrate.

The step of packaging the separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate in a package body includes the step of molding the package body around a leadframe, the integrated-circuit die and the separate silicon substrate to which the integrated-circuit die is fixed. The step of packaging the separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate in a package body includes the steps of providing a cavity in a cavity-type package with a mounting surface formed adjacent to the cavity and fixing the separate silicon substrate to the mounting surface. The step of attaching connection wires from the integrated-circuit die or the leadframe to at least one interposer area formed on the top surface of the silicon substrate.

The invention further includes the step of attaching connection wires from the integrated-circuit die or the leadframe to at least one interposer area formed on the top surface of the silicon substrate. The step of attaching connection wires from the integrated-circuit die or the leadframe to at least one interposer area formed on the top surface of the silicon substrate includes attaching connection wires to the at least one interposer which extends between the integrated circuit die and the top surface of the silicon substrate. The method also includes the step of attaching the connection wires to a layer of conductive material which is formed over a layer of oxide formed on the surface of the silicon substrate.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIGURE 1 is a sectional view of a package assembly with an integrated-circuit die mounted to a separate heat conductive silicon substrate, where the separate heat conductive silicon substrate is mounted to the die-attach pad of a lead frame.

FIGURE 2 is a sectional view of a package assembly with an integrated-circuit die mounted to a separate heat conductive silicon substrate, which is used as the die-attach pad portion of a lead frame.

FIGURE 3 is a sectional view of a package assembly similar to the assembly of Figure 2 and further including interposers, or connections areas, formed on the surface of the silicon substrate.

FIGURE 4 is a sectional view of a package assembly similar to the assembly of Figure 3 where the interposers extend under the integrated-circuit die.

FIGURE 5 is a sectional view of a package assembly similar to the assembly of Figure 4 where the interposers have more than one conductive layer formed thereon.

FIGURE 6 is a sectional view of a package assembly in which a separate silicon substrate is mounted within a cavity formed in a ceramic pin grid array (PGA) package body having a number of conductive layers formed therein.

FIGURE 7 is a sectional view of a package assembly in which a separate silicon substrate is mounted within a cavity formed in the ceramic PGA package body of Figure 6 and which further includes interposers, or connections areas, formed on the surface of the silicon substrate.

FIGURE 8 is a sectional view of a package assembly similar to the assembly of Figure 7 where the interposers extend under the integrated-circuit die.

FIGURE 9 is a sectional view of a package assembly similar to the ceramic PGA package assembly of Figure 8 with the addition of multi-layer interposers being formed on the top surface of the silicon substrate.

FIGURE 10 is a sectional view of a PGA package assembly in which a separate silicon substrate is mounted within a cavity formed in a package body, which is fabricated as a multi-layer printed-circuit board with a number of conductive layers formed therein.

FIGURE 11 is a sectional view of the PGA package assembly of Figure 10 in which a separate silicon substrate is mounted within a cavity formed in a multi-layer printed circuit package body and which further includes interposers, or connections areas, formed on the surface of the silicon substrate.

FIGURE 12 is a sectional view of a PGA package assembly with the multi-layer printed circuit package body similar to the assembly of Figure 11 where the interposers extend under the integrated-circuit die.

FIGURE 13 is a sectional view of a PGA package assembly similar to the package assembly of Figure 12 with the

addition of multi-layer interposers being formed on the top surface of the silicon substrate.

FIGURE 14 is an enlarged, sectional view of a portion of the PGA package assembly of Figure 13 showing typical interconnections between various external package pins and various conductive layers in the package body.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

FIGURE 1 shows a package assembly 10 provided according to the invention for a package having a molded body. The package assembly 10 has the bottom surface of an integrated-circuit die 12 mounted to the top surface of a separate heat conductive silicon substrate 14 using a thin layer 16 of die-attach material. The die-attach material is a standard epoxy die-attach material, which is thermally conductive and which is made electrically conductive by adding, for example, silver or another conductive material.

In this embodiment of the invention, the separate heat conductive silicon substrate 14 is fixed with a layer of suitable adhesive material 18 to a die-attach pad 20 of a leadframe. The leadframe has leads which extend inwardly towards a central region of the leadframe. The leads have bonding fingers 22 formed at the inward ends thereof. Bonding wires 24 extend from the wire-bonding pads 26 formed on the top surface of the integrated circuit die 12 to the bonding fingers 22, as indicated in the Figure.

As shown in the Figure, the silicon substrate 14 is a separate piece which can have lateral dimensions greater than the lateral dimensions of the integrated-circuit die 12. The

separate silicon substrate 14 functions as a heat sink or heat spreader to enhance the thermal performance of the package assembly 10. The separate silicon substrate 14 is also available to be used as a single or multi-layer interposer.

Use of silicon as a substrate material has certain advantages. Silicon as a substrate material is inexpensive and readily available for the application described herein below as reject wafers from an integrated-circuit fabrication line. Silicon is thermally matched to the package components. The characteristics of the silicon substrate match those of the integrated-circuit die. Crystalline silicon has good temperature characteristics. Silicon also has the advantage that depositing of conductors on its surface is readily accomplished using standard integrated-circuit, multi-layer-metal technology. The thermal coefficient of expansion mismatches internal to a package are the same as those in current package designs. Finally, existing packaging materials and technologies can be used.

FIGURE 2 shows another molded-package assembly 30 which includes an integrated-circuit die 32 mounted to the top surface of a separate heat conductive silicon substrate 34 using a thin layer 36 of die-attach material. The die-attach material is a standard epoxy die-attach material, which is thermally conductive and which, if necessary, is made electrically conductive by adding, for example, silver or another conductive material.

In this embodiment, no die-attach pad is used. Bonding fingers 42 formed at the inward ends of leads of a leadframe are fixed with a layer 44 of substrate-attach material to the peripheral areas of the top surface of the separate heat conductive silicon substrate 34. Bonding wires 46 extend from wire-bonding pads 48 formed on the top surface of the

integrated-circuit die 32 to the bonding fingers 42, as indicated in the Figure.

FIGURE 3 shows a molded-package assembly 50, which is similar to the assembly of Figure 2 so that the same reference numerals are used for like elements. This embodiment of the invention includes interposers 60, or connections areas, which are conveniently formed on the surface of the silicon substrate. The interposers are formed of conductive material such as, for example, aluminum deposited on the top surface of the silicon substrate 34. The interposers are formed with various shapes, including, for example, elongated strips extending from near the integrated-circuit die 32 to the peripheral areas on the top surface of the silicon substrate 34.

Bonding wires 62 extend from the wire-bonding pads 48 formed on the top surface of the integrated-circuit die 32 to the inner ends of the interposers 60 near the integrated-circuit die 32 as indicated in the Figure. The outer ends of the interposers 60 are connected by bonding wires 64 to the bonding fingers 42, as indicated in the Figure.

FIGURE 4 shows a molded-package assembly 70, which is similar to the assembly of Figure 3, so that the same reference numerals are used for like elements. In this embodiment, interposers 72 are provided which extend under the integrated-circuit die 32, as shown in the Figure. This arrangement accommodates various die sizes so that a standard package is provided for a wide range of die sizes. This type of package configuration is particularly useful in an environment where limited production runs of different die sizes are to be run. Only one or a small number of different standard package configurations must then be inventoried.

With this embodiment of the invention, various sizes of integrated-circuit dies 32 are accommodated. Bonding wires 74 from the bonding pads 48 on a particular die 32 are bonded near the die 32, as indicated in the Figure. For different die sizes, the bonding location on the interposer 72 will vary, depending upon the size of the die. Thus, for a die larger than the die shown, bonding sites on the interposer 72 will be closer towards the periphery of the silicon substrate 34.

FIGURE 5 shows another embodiment of a molded-package assembly which is similar to the assembly of Figure 4, so that the same reference numerals are used for like elements. In this embodiment, the interposers 72 extend under the integrated-circuit die 32, as shown in the Figure to accommodate a range of various die sizes. This type of package configuration is particularly useful in an environment where limited production runs of somewhat different die sizes are to be run.

In this embodiment, an insulation layer 82 is formed over the interposers 72. The insulation layer is formed, for example, as a layer 82 of oxide material deposited on the surface of the silicon substrate 72. The layer of oxide 82 has a layer 84 of conductive material formed on its top surface. These alternate layers of insulating material can be repeated, as desired. Various portions of conductive layers can be exposed and made available for connections.

Various wire-bond connections are available with this configuration. A bonding wire 86 is connected between the bonding finger 42 and the interposer 72. A bonding wire 88 is connected between the bonding pad 48 on the integrated- circuit die 32 and the interposer 72. A bonding wire 90 is connected between another bonding pad 48 on the integrated- circuit die 32 and the conductive layer 84. Another bonding wire 92 is

connected between the conductive layer 84 and a bonding finger 42.

FIGURE 6 shows a pin-grid-array (PGA) package assembly 100 in which a separate silicon substrate 102 is mounted within a cavity 104 formed in a cavity-type package body 106 formed of a ceramic material. The cavity is covered with a lid member 107 which is fixed to the ceramic package body 106 with a layer of an appropriate material. The package body 106 has number of conductive layers (typically shown as 108) formed therein. Internal connections (not shown) are conventionally provided between various ones of the conductive layers 108 and respective ones of the external package pins (typically shown as 109).

A mounting surface 110 for the separate silicon substrate 102 is formed on the base portion of the ceramic PGA package body adjacent to the cavity 104, as indicated in the Figure. The separate silicon substrate 102 is mounted to the mounting surface 104 with a thin layer 112 of suitable substrate-attachment material. This material can be a standard epoxy material, which is thermally conductive and which is made electrically conductive by adding, for example, silver or another conductive material.

The separate silicon substrate 102 also serves as a die-attach pad for an integrated-circuit die 114 which is attached to the top surface of the separate silicon substrate 102 with a thin layer 116 of die-attach material. Wire-bonded bonding wires 118, 119 typically extend from wire-bonding pads formed on the top surface of the integrated-circuit die 114 to various exposed portions of the conductive layers 108, as indicated in the Figure.

FIGURE 7 shows another embodiment of a PGA ceramic package assembly 120, which is similar to the assembly of Figure 6, so that the same reference numerals are

used for like elements. The separate silicon substrate 102 is mounted within the cavity formed within the ceramic PGA package body 106. In this case the package assembly 120 further includes interposers 122, 123, or conductive connection areas, formed on the upper surface of the silicon substrate 102, as illustrated.

The interposers 122, 123 provide intermediate connections areas so that shorter bonding wires can be used, in comparison to the longer bonding wires 118, 119 of Figure 6. Wire-bonded bonding wires 124, 125 extend between bonding pads formed on the top surface of the integrated-circuit die 114 and various portions of the interposers 122, 123, as indicated in the Figure. Shorter bonding wires 126, 127 extend respectively between from the outer areas of the interposers 122, 123 to various exposed portions of the conductive layers 108, as indicated in the Figure.

FIGURE 8 shows a sectional view of another embodiment of a package assembly 130 which is very similar to the assembly of Figure 7 so that the same reference numerals are used for like elements. In this case, interposers 132, 134 extend beneath the die 114, as illustrated. This permits a number of different die sizes to be accommodated by one package configuration.

FIGURE 9 shows a sectional view of an embodiment of a package assembly 140 which is very similar to the assembly of Figure 8 so that the same reference numerals are used for like elements. In this case the interposers have additional conductive layers 142, 143 formed over respective layers 144, 146 of oxide formed on the surface of the silicon substrate. These additional conductive layers 142, 143 are used, for example, as connection areas for a bonding wire 146 from a bonding pad on the die 114 or for a bonding wire 148 from one of the conductive layers 108 of the package body 106.

Additional alternate layers of oxide and conductive material can be formed to provide additional intermediate connection areas, as required for particular applications, to provide multi-layer interposers on the top surface of the silicon substrate 102.

FIGURES 10-13 illustrate PGA package assemblies which use a package body 150, which is fabricated as a multi-layer printed-circuit board with a number of conductive layers 152 formed therein. These package assemblies are similar to the ceramic package assemblies illustrated in Figures 6-10.

FIGURE 10 illustrates a pin-grid-array (PGA) package assembly 160 in which a separate silicon substrate 162 is mounted within a cavity 164 formed in the cavity-type package body 150, which is formed as a multi-layer printed-circuit board. The cavity is covered with a lid member 167 which is fixed to the ceramic package body 150 with a layer of an appropriate material. The package body 150 has the number of conductive layers (typically shown as 152) formed therein. Internal connections (not shown) are conventionally provided between various ones of the conductive layers 152 and respective ones of the external package pins (typically shown as 168).

A mounting surface 170 for the separate silicon substrate 162 is formed on the base portion of the multi-layer printed-circuit board PGA package body adjacent to the cavity 164, as indicated in the Figure. The separate silicon substrate 162 is mounted to the mounting surface 170 with a thin layer 172 of suitable substrate-attachment material. This material can be a standard epoxy material, which is thermally conductive and which is made electrically conductive by adding, for example, silver or another conductive material.

The separate silicon substrate 162 also serves as a die-attach pad for an integrated-circuit die 174 which is attached to the top surface of the separate silicon substrate 162 with a thin layer 176 of die-attach material. Wire-bonded bonding wires 178, 179 typically extend from wire-bonding pads formed on the top surface of the integrated-circuit die 174 to various exposed portions of the conductive layers 152, as indicated in the Figure.

FIGURE 11 shows a sectional view of another embodiment of a multi-layer printed-circuit board package assembly 180 which is very similar to the assembly of Figure 10, so that the same reference numerals are used for like elements. In this case, interposers 182, 183 extend beneath the die 174, as illustrated. This permits a number of different die sizes to be accommodated by one package configuration.

The interposers 182, 183 provide intermediate connections areas so that shorter bonding wires can be used, in comparison to the longer bonding wires 178, 179 of Figure 10. Wire-bonded bonding wires 184, 185 extend between bonding pads formed on the top surface of the integrated-circuit die 174 and various portions of the interposers 182, 183, as indicated in the Figure. Shorter bonding wires 186, 187 extend respectively between from the outer areas of the interposers 182, 183 to various exposed portions of the conductive layers 152, as indicated in the Figure.

FIGURE 12 shows a sectional view of another embodiment of a multi-layer printed circuit body package assembly 190 which is very similar to the assembly of Figure 11 so that the same reference numerals are used for like elements. In this case, interposers 182, 184 extend beneath the die 174, as illustrated. This permits a number of different die sizes to be accommodated by one package configuration.

FIGURE 13 shows a sectional view of an embodiment of a multi-layer printed circuit body package assembly 200 which is very similar to the assembly of Figure 12 so that the same reference numerals are used for like elements. In this case the interposers have additional conductive layers 202, 203 formed over respective layers 204, 205 of oxide formed on the surface of the silicon substrate. These additional conductive layers 202, 203 are used, for example, as connection areas for a bonding wire 206 from a bonding pad on the die 174 or for a bonding wire 208 from one of the conductive layers 152 of the package body 150.

Additional alternate layers of oxide and conductive material can be formed to provide additional intermediate connection areas, as required for particular applications, to provide multi-layer interposers on the top surface of the silicon substrate 162.

FIGURE 14 shows a portion of the PGA package assembly 200 of Figure 13, illustrating typical interconnections between various typical external package pins 168 and various typical conductive layers 152 in the package body. In this case, plated-through holes 210, 212 are typically shown extending through the body of the package to provide conductive connections between the conductive layers 1152 and the external package pins 168.

Using the interposer with the separate silicon substrate provides for assembly of a very small die in a high pincount packages. The separate silicon substrate allows an integrated-circuit die to be bonded out in a standard package bond-out configuration and in a universal bond-out configuration without crossing wires.

As a bare substrate attached to a leadframe of a molded-plastic package, the invention provides a very cost effective solution for thermal enhancement of the package.

The separate silicon substrate could be patterned using existing integrated-circuit fabrication and processing technology to provide an interposer. The interposer reduces the wirelengths required for a die with a limited number pads in a high pincount packages. The interposer uses single level metalization techniques known in the art of fabricating integrated circuits.

If triple-layer metal patterning techniques are used on the separate silicon substrate, the invention could also be used to duplicate the pinout of an electrical and thermally enhanced with a standard metric quad flat pack (MQFP) package or a molded-plastic thermally enhanced package. If triple-layer metal patterning techniques are used on the separate silicon substrate provided according to the invention, the invention could also be used to duplicate the pinout of either an 8-layer high performance ceramic pin grid array (HPCPGA) or an 8-layer high performance plastic pin grid array (HPPPGA) package in a 5-layer high performance ceramic pin grid array (HPCPGA) or a 5-layer high performance plastic pin grid array HPPPGA package. These configuration reduce the number of required package layer from 8 to 5.

The separate silicon substrate according to the invention could also be patterned to allow for attachment of multiple integrated-circuit dies to the separate silicon substrate.

Standard techniques are employed in practicing the invention. An integrated circuit die is attached to a silicon substrate with standard epoxy die-attach material, which is thermally conductive and which is made electrically conductive by adding, for example, silver. For ceramic or

plastic pin grid array (PPGA) multi-layer packages, these same epoxy attachment techniques are used. Silicon as a substrate material is inexpensive and readily available as reject wafers from integrated-circuit fabrication lines. Crystalline silicon has good temperature characteristics. Depositing of conductors is readily accomplished using integrated-circuit multi-layer-metal technology.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular us contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

IN THE CLAIMS:

1. An integrated-circuit package assembly, comprising:

an integrated-circuit die;

a separate silicon substrate having a top surface and a bottom surface, said integrated-circuit die being fixed to said top surface of said separate silicon substrate, said separate silicon substrate serving as a heat spreader for said integrated-circuit die;

a package body containing said separate silicon substrate with said integrated-circuit die fixed to said separate silicon substrate.

2. The integrated-circuit package assembly of Claim 1 further comprising:

said package body being a molded package body which is formed around a leadframe, said integrated-circuit die and said separate silicon substrate to which said integrated-circuit die is fixed;

said leadframe having leads extending inwardly towards a central region of said leadframe, said leads having bonding fingers formed at the inward ends thereof.

3. The integrated-circuit package assembly of Claim 2 further comprising said bonding fingers being attached to said separate silicon substrate.

4. The integrated-circuit package assembly of Claim 3, wherein said lead frame has a die-attach pad portion to which is fixed said separate silicon substrate.

5. The integrated-circuit package assembly of Claim 2, wherein said separate silicon substrate has lateral dimensions greater than the lateral dimensions of said integrated-circuit die and wherein at least one interposer area is formed on said top surface of said silicon substrate for attachment of connection wires from said integrated-circuit die or said leadframe.

6. The integrated-circuit package assembly of Claim 5 wherein a portion of said at least one interposer is formed on said top surface of said separate silicon substrate extends between said integrated circuit die and said top surface of said silicon substrate.

7. The integrated-circuit package assembly of Claim 5 wherein a portion of said at least one interposer which is formed on said top surface of said silicon substrate extends between the bottom surface of said integrated circuit die and said top surface of said silicon substrate to accommodate integrated-circuit dies of various sizes.

8. The integrated-circuit package assembly of Claim 1, wherein said at least one interposer is formed as a layer of oxide formed on said top surface of said silicon substrate, which layer of oxide is covered with a layer of conductive material.

9. The integrated-circuit package assembly of Claim 8, wherein said at least one interposer is formed as a layer of oxide formed on said top surface of said silicon substrate, over which another layer of oxide and conductive material is formed.

10. The integrated-circuit package assembly of Claim 1 wherein said package body is a cavity-type package body having a cavity formed therein, wherein said package body includes a mounting surface formed adjacent to said cavity, and wherein said mounting surface has said separate silicon substrate fixed thereto.

11. The integrated-circuit package assembly of Claim 10 wherein at least one interposer is formed on said top surface of said separate silicon substrate for connection of wires from said integrated-circuit die or said cavity-type package body.

12. The integrated-circuit package assembly of Claim 11 wherein a portion of said at least one interposer is formed on said top surface of said silicon substrate extends between said integrated circuit die and said top surface of said silicon substrate to accommodate integrated-circuit dies of various sizes.

13. The integrated-circuit package assembly of Claim 11 wherein said connections are wire-bonded wires.

14. The integrated-circuit package assembly of Claim 11 wherein said at least one interposer is formed as a layer of oxide formed on said surface of said silicon substrate, which layer of oxide is covered with a layer of conductive material.

15. The integrated-circuit package assembly of Claim 14, wherein said at least one interposer is formed as a layer of oxide formed on said top surface of said silicon substrate, over

which alternate layers of oxide and conductive material are formed.

16. The integrated-circuit package assembly of Claim 14, wherein said package body is formed of a ceramic material.

17. The integrated-circuit package assembly of Claim 14, wherein said package body is formed as a printed-circuit board structure.

18. An integrated-circuit package assembly, comprising:

an integrated-circuit die;

a leadframe having leads extending inwardly towards a central region of said leadframe, said leads having bonding fingers formed at the inward ends thereof;

a separate silicon substrate having a top surface and a bottom surface, said integrated-circuit die being mounted on said top surface of said separate silicon substrate, said separate silicon substrate serving as a heat spreader for said integrated-circuit die;

a molded package body which contains said separate silicon substrate with said integrated-circuit die mounted thereto and which is formed around a leadframe, said integrated-circuit die and said separate silicon substrate.

19. The integrated-circuit package assembly of Claim 18, wherein said separate silicon substrate has lateral dimensions greater than the lateral dimensions of said integrated-circuit die and wherein at least one interposer area is formed on said top surface of said silicon substrate for attachment of connection wires from said integrated-circuit die or said leadframe.

20. The integrated-circuit package assembly of Claim 19 wherein a portion of said at least one interposer is formed on said top surface of said separate silicon substrate extends between said integrated circuit die and said top surface of said silicon substrate.

21. The integrated-circuit package assembly of Claim 19, wherein said at least one interposer is formed as a layer of oxide formed on said surface of said silicon substrate, which layer of oxide is covered with a layer of conductive material.

22. An integrated-circuit package assembly, comprising:

an integrated-circuit die;

a separate silicon substrate having a top surface and a bottom surface, said integrated-circuit die being mounted on said top surface of said separate silicon substrate, said separate silicon substrate serving as a heat spreader for said integrated-circuit die;

a package body having a cavity formed therein with a mounting surface formed in said package body adjacent to said cavity, wherein said mounting surface has said separate silicon substrate mounted thereto.

23. The integrated-circuit package assembly of Claim 22 wherein at least one interposer is formed on said top surface of said silicon substrate for connections of wires from said integrated-circuit die or said cavity-type package body.

24. The integrated-circuit package assembly of Claim 23 wherein a portion of said at least one interposer is formed on said top surface of said silicon substrate extends between said

integrated circuit die and said top surface of said silicon substrate.

25. The integrated-circuit package assembly of Claim 23 wherein said at least one interposer is formed as a layer of oxide formed on said top surface of said silicon substrate, which layer of oxide is covered with a layer of conductive material.

26. The integrated-circuit package assembly of Claim 22, wherein said package body is formed of a ceramic material.

27. The integrated-circuit package assembly of Claim 22, wherein said package body is formed as a printed-circuit board structure.

28. A method of cooling an integrated-circuit die, comprising the steps of:

fixing the integrated circuit die to the top surface of a separate silicon substrate having a top surface and a bottom surface,

packaging the separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate in a package body; and

conducting heat from the integrated-circuit die using the separate silicon substrate.

29. The method of Claim 28 wherein the step of packaging the separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate in a package body includes the step of molding the package body around a

leadframe, the integrated-circuit die and the separate silicon substrate to which the integrated-circuit die is fixed.

30. The method of Claim 28 wherein the step of packaging the separate silicon substrate with the integrated-circuit die fixed to the separate silicon substrate in a package body includes the steps of providing a cavity in a cavity-type package with a mounting surface formed adjacent to the cavity and fixing the separate silicon substrate to the mounting surface.

31. The method of Claim 28 including the step of attaching connection wires from the integrated-circuit die or the leadframe to at least one interposer area formed on the top surface of the silicon substrate.

32. The method of Claim 28 including the step of attaching connection wires from the integrated-circuit die or the leadframe to at least one interposer area formed on the top surface of the silicon substrate.

33. The method of Claim 32 where the step of attaching connection wires from the integrated-circuit die or the leadframe to at least one interposer area formed on the top surface of the silicon substrate includes attaching connection wires to the at least one interposer which extends between the integrated circuit die and the top surface of the silicon substrate.

34. The method of Claim 32 including the step of attaching the connection wires to a layer of conductive material which is formed over a layer of oxide formed on the surface of the silicon substrate.

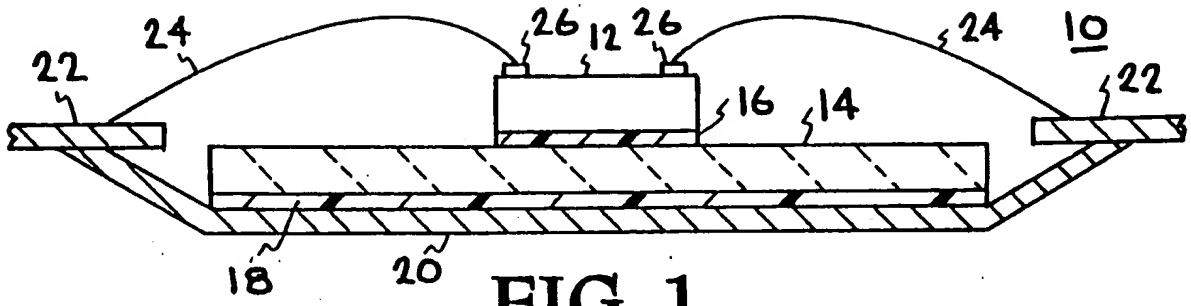


FIG. 1

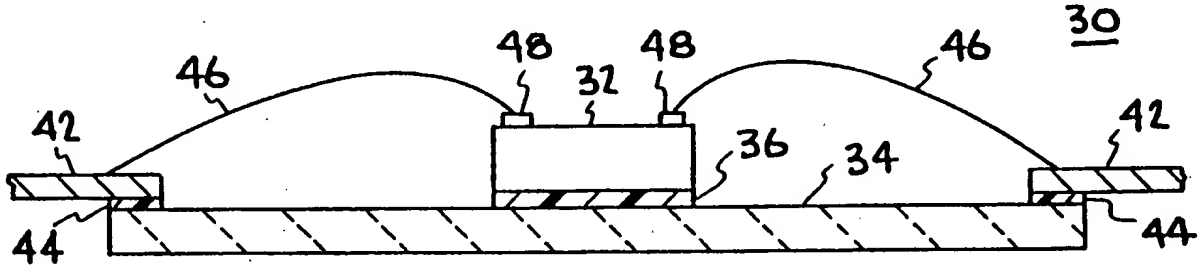


FIG. 2

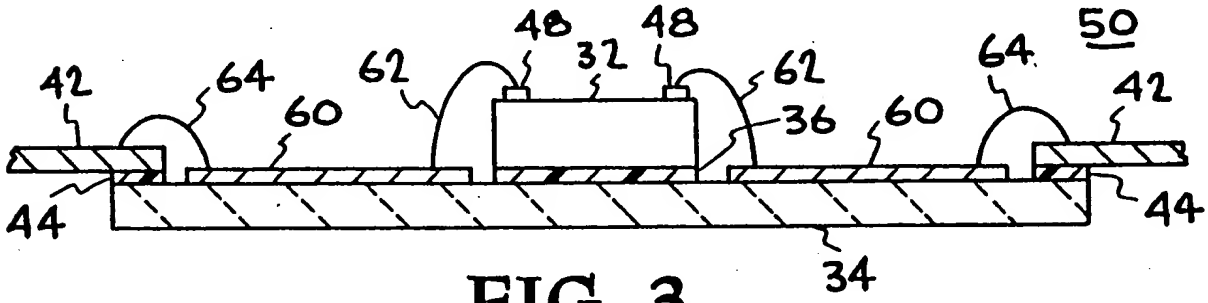


FIG. 3

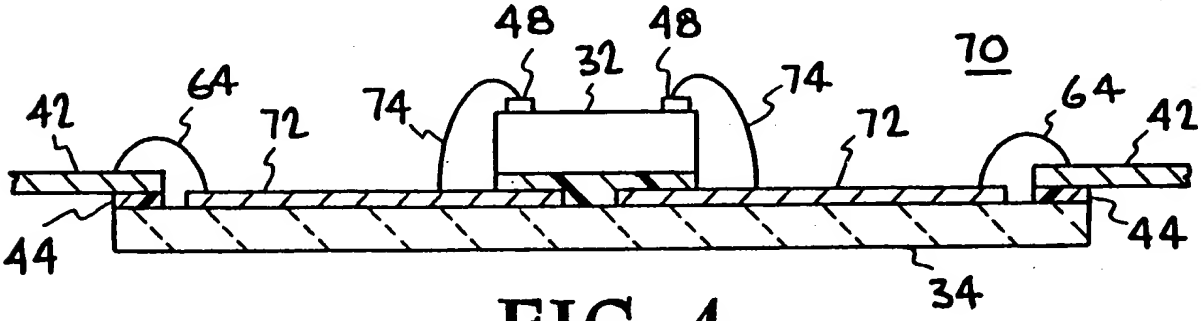


FIG. 4

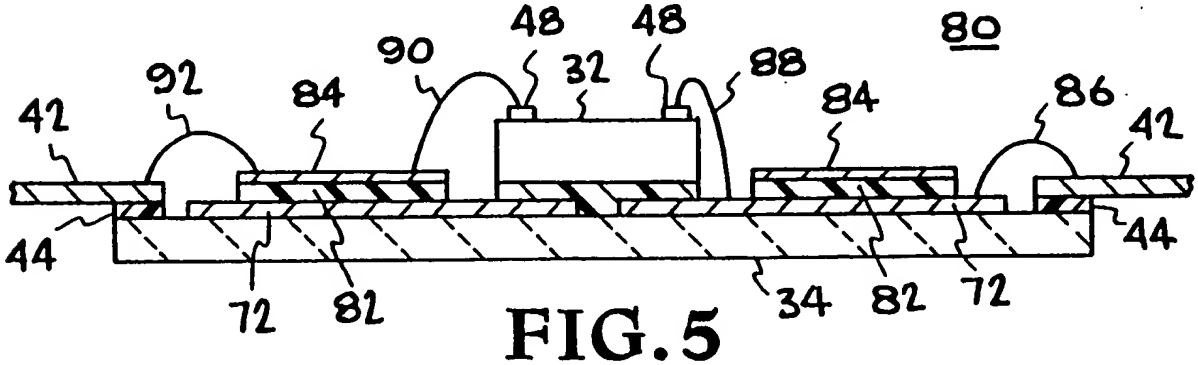


FIG. 5

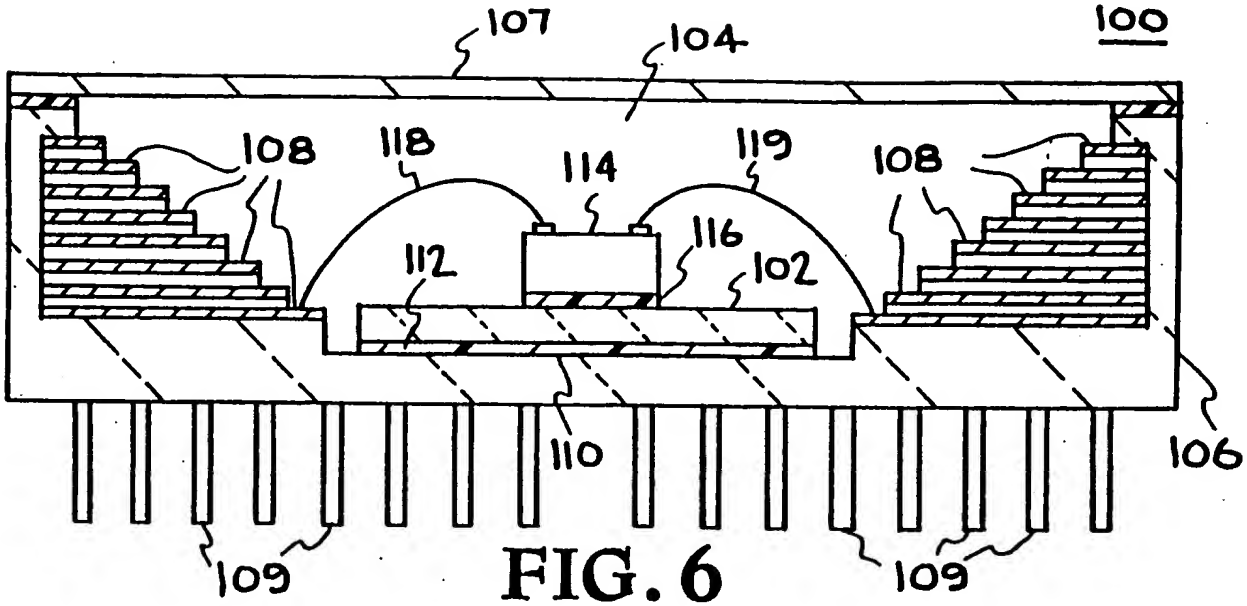


FIG. 6

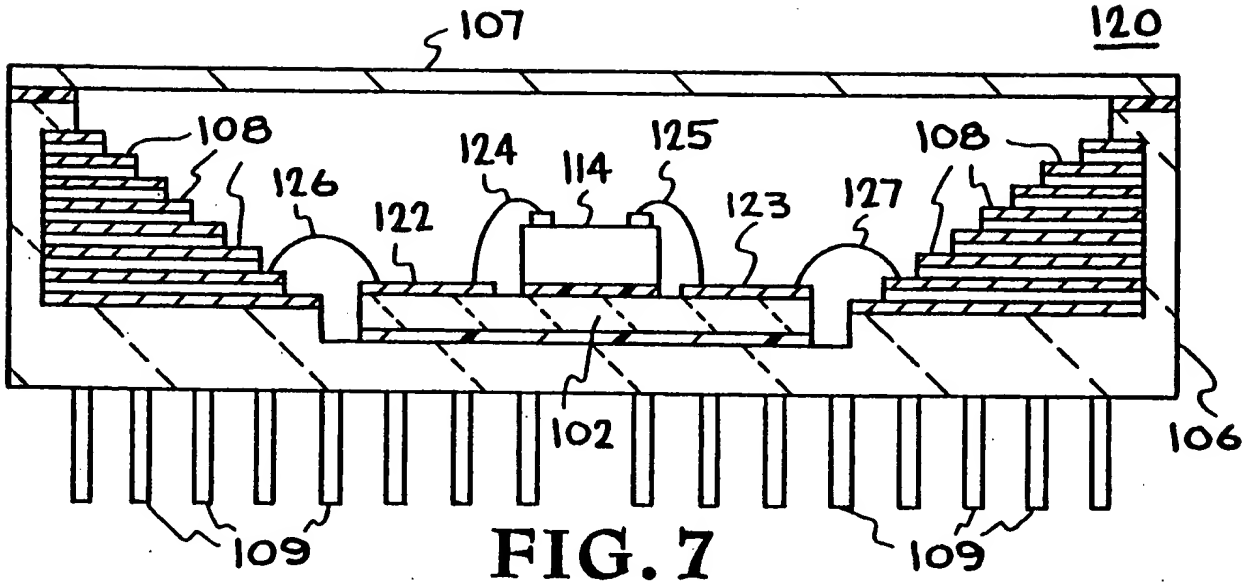


FIG. 7

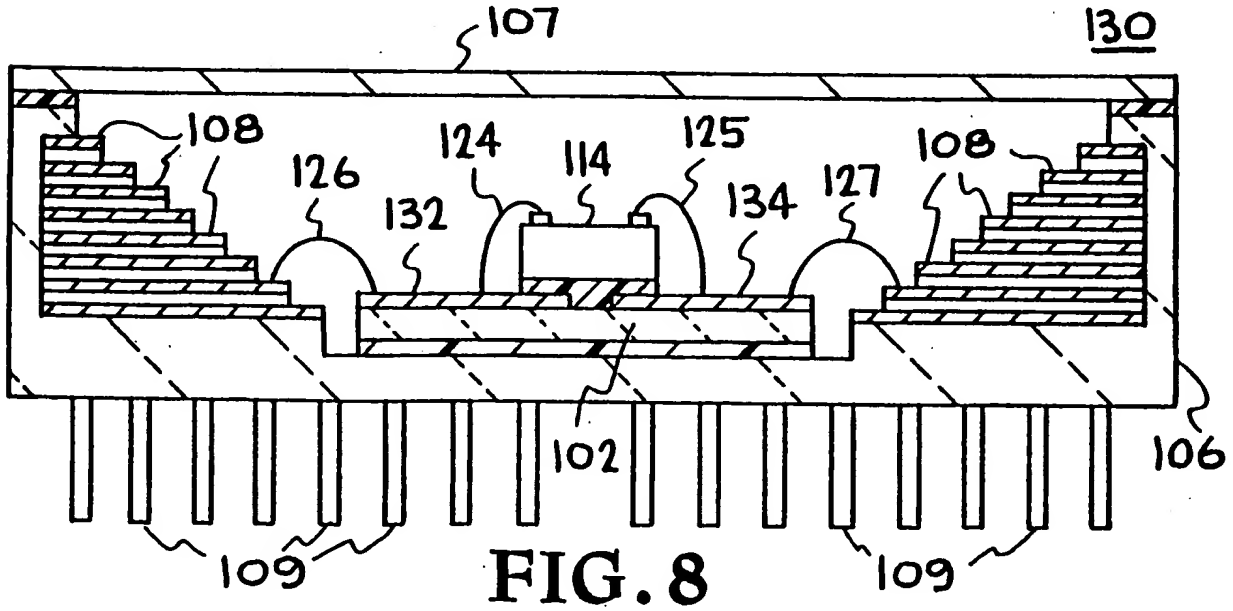


FIG. 8

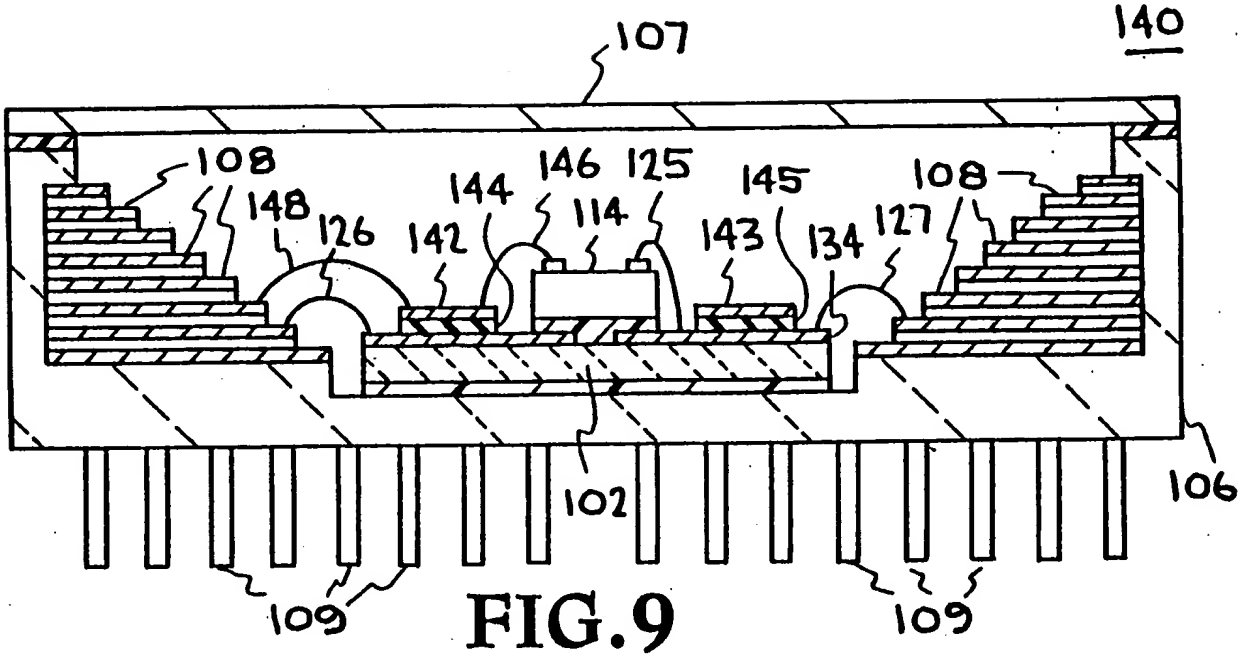


FIG.9

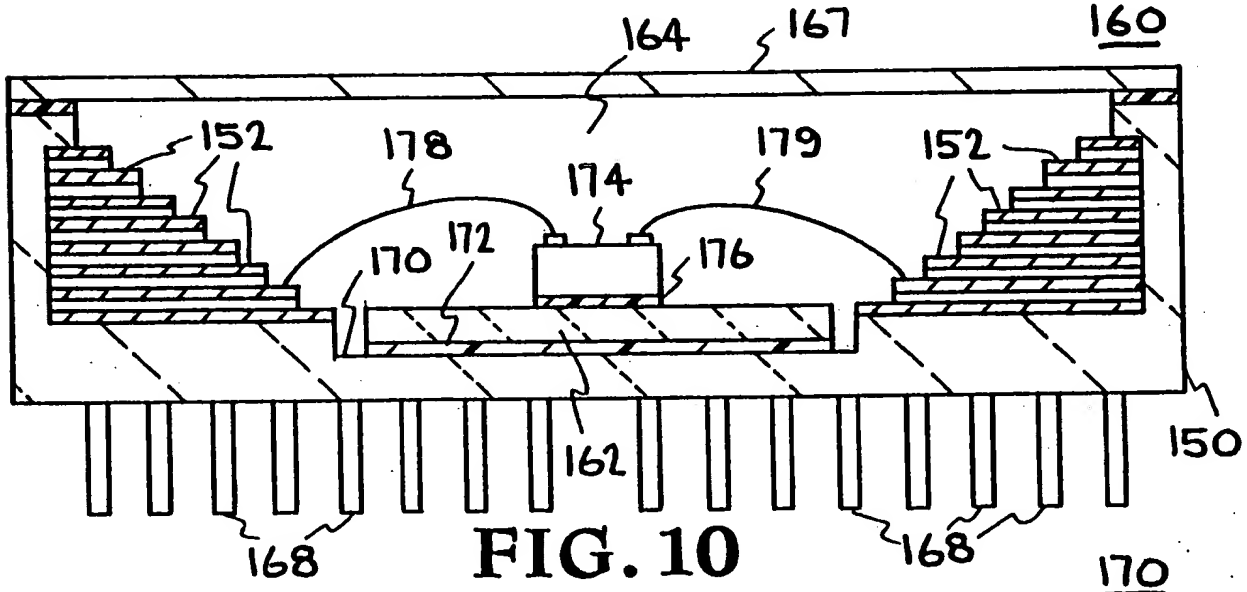


FIG. 10

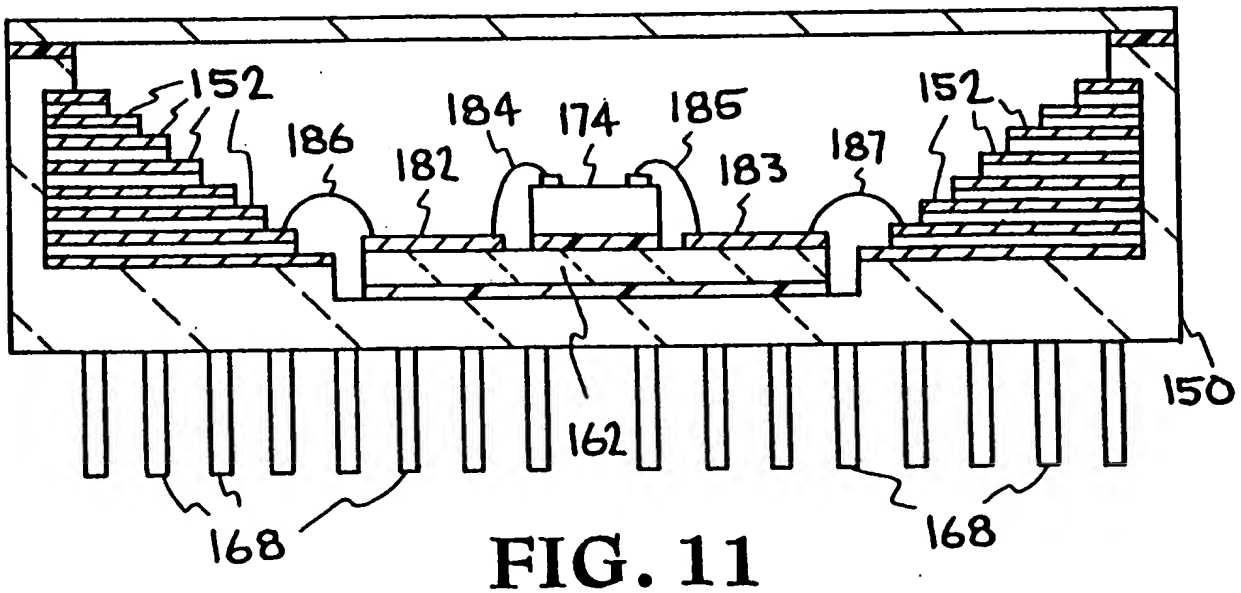


FIG. 11

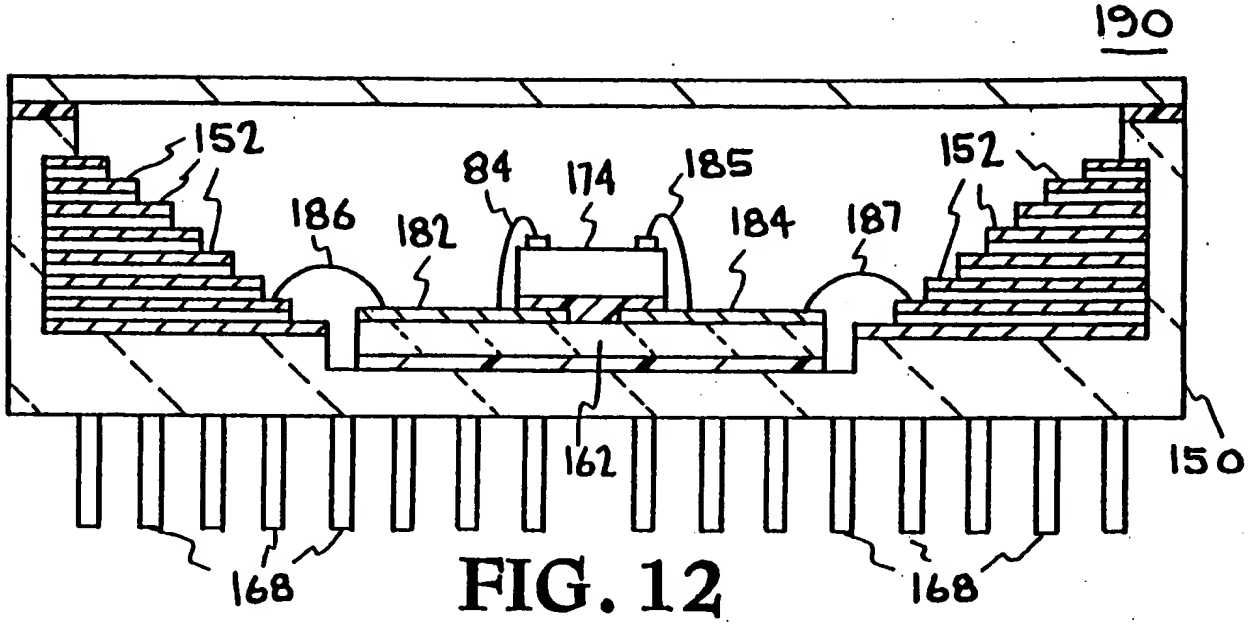


FIG. 12

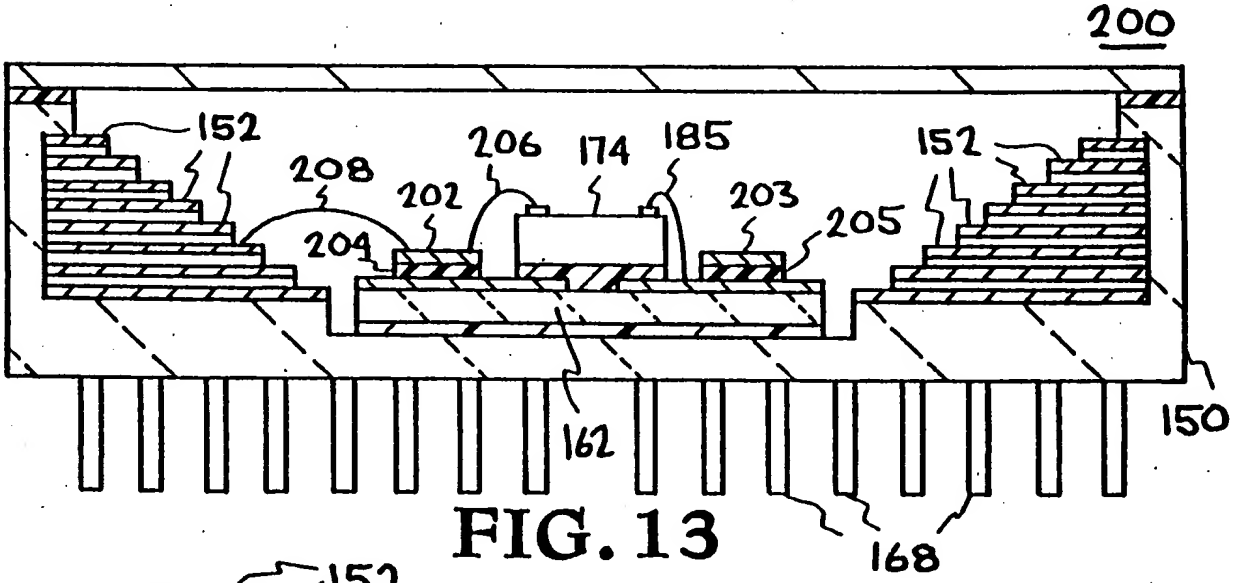


FIG. 13

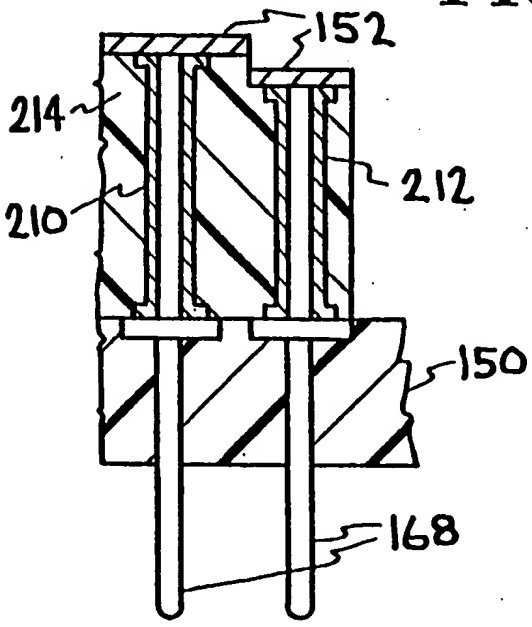


FIG. 14

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/06739

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H01L23/495 H01L23/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y | FR,A,2 684 803 (GEMPLUS CARD INTERNATIONAL) 11 June 1993<br>see page 4, line 14 - page 5, line 23;<br>figures 3,6,10 | 1,2,4,<br>18,28,29<br>3,5-16,<br>19-21,<br>31-34 |
| | --- | |
| Y | PATENT ABSTRACTS OF JAPAN<br>vol. 012, no. 221 (E-625) 23 June 1988<br>& JP,A,63 015 447 (NEC CORP) 22 January 1988<br>see abstract | 5-7,<br>10-12,<br>19,20,<br>31-33 |
| | --- | |
| Y | PATENT ABSTRACTS OF JAPAN<br>vol. 006, no. 012 (E-091) 23 January 1982<br>& JP,A,56 134 747 (MITSUBISHI ELECTRIC CORP.) 21 October 1981<br>see abstract | 8,9,<br>13-16,<br>21,34 |
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[X] Further documents are listed in the continuation of box C.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 October 1994 | 14. 11. 94 |
| **Name and mailing address of the ISA**<br>European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | **Authorized officer**<br>Zeisler, P |

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International application No.
PCT/US 94/06739

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | EP,A,0 509 825 (NEC CORPORATION) 21 October 1992<br>see column 5, line 3 - line 16; figure 1 | 9,15 |
| Y | EP,A,0 520 679 (AMERICAN TELEPHONE & TELEGRAPH COMPANY) 30 December 1992 | 3 |
| A | see the whole document | 10-15 |
| X | EP,A,0 516 185 (HITACHI LTD) 2 December 1992 | 1,22-26 |
| A | see column 12, line 29 - column 16, line 50; figures 3C,3D | 10-16 |
| P,A | WO,A,93 20586 (VLSI TECHNOLOGY INC) 14 October 1993 | |
| P,A | WO,A,93 17455 (VLSI TECHNOLOGY INC) 2 September 1993 | |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US 94/06739

| Patent document cited in search report | Publication date | Patent family member(s) | | Publication date |
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| | | US-A- | 5309011 | 03-05-94 |
| WO-A-9320586 | 14-10-93 | NONE | | |
| WO-A-9317455 | 02-09-93 | JP-T- | 6507276 | 11-08-94 |

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